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09/768,665	01/24/2001	Tuyet-Huong Thi Nguyen	016295.0624	3786
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Roger Fulghum Baker & Butts, L.L.P. One Shell Plaza 910 Louisiana Houston, TX 77002-4995		EXAMINER DANG, KHANH		
		ART UNIT 2111		PAPER NUMBER
SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE		
3 MONTHS	12/27/2006	PAPER		

**Please find below and/or attached an Office communication concerning this application or proceeding.**

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

## Office Action Summary

**Application No.**

09/768,665

**Applicant(s)**

NGUYEN ET AL.

**Examiner**

Khanh Dang

**Art Unit**

2111

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 23 October 2006.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1, 4-8, 16 and 19-23 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1, 4-8, 16, and 19-23 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
  - ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- |  |   |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)   | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                       | 5) <input type="checkbox"/> Notice of Informal Patent Application                       |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

**DETAILED ACTION**

***Notice to Applicants***

**This application, previously assigned to and examined by Ex. King, is now assigned to Ex. Dang. Any future contact should be directed to Ex. Khanh Dang whose contact information is provided below.**

**Since Applicants do not amend the claims, the previous Office Action issued by Ex. King is reproduced above with added explanation for clarification, provide by Ex. Dang, underlined.**

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 1, 4-8, 16, and 19-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over the admitted prior art in view of Goodman et al. (U.S. Patent No. 6,282,601) and Smith et al. (U.S. Patent No. 3,643,227).

Referring to claim 1: The admitted prior art discloses writing parameters for the SMI routines to a predetermined register of a first processor (Specification, page 3, lines 4-6), executing in the first processor a command of a software application to cause the first processor to initiate a system management interrupt (Specification, page 2, lines 8-17), receiving at each processor an instruction that the system management interrupt has been issued (Specification, page 2, lines 19-20), entering system management mode at each processor (Specification, page 2, lines 20-21), and saving register contents of each processor to a memory space associated with each respective processor (Specification, page 2, lines 22-24). The admitted prior art's parameters for the SMI routines are the claimed predetermined signature.

The admitted prior art further discloses that a different processor, other than the processor initiating the interrupt, may be selected for handling the interrupt (Specification, page 3, lines 13-16); thus, the admitted prior art discloses selecting from among the multiple processors a second processor as a system management interrupt handler. **Note that to select is to choose in preference to another or others. Note also that selection must be based on specific criteria. Thus, it is clear that selection based on specific criteria is selection based on an arbitration scheme. In any event, as already indicated by Ex. King, the use of arbitration scheme in general is old and well-known as evidenced by at least Smith.**

Neither the admitted prior art discloses selecting the second processor according to an arbitration scheme nor the admitted prior art discloses scanning the content of the memory for the selected second processor to process the interrupt.

Goodman discloses an interrupt handling method in a multiprocessor environment. Goodman discloses scanning the content of the memory for the selected second processor to process the interrupt (figure 4, steps 126, 128, and 130); and when the second processor locates the saved predetermined signature in one of the memory spaces associated with the processors of the computers system, using the contents of the memory space associated with the predetermined signature for any parameters necessary for the handling of the system management interrupt (figure 4, steps 134, 136, and 138). Goodman teaches one to identify the requesting processor without having to satisfy severe interrupt timing constraint (column 1, lines 66-67, column 2, lines 1-5). Although Goodman discloses and teaches one to scan the processor register in handling interrupt, Goodman does not explicitly disclose an arbitration scheme in selecting one processor to execute the interrupt.

Smith discloses assigning tasks to the idle processor (abstract). Smith teaches one to distribute the task to the processor based on the processor's current workload.

Hence, it would have been obvious to one having ordinary skill in the computer art to adapt the teachings of Goodman and Smith onto the admitted prior art because Goodman teaches one to identify the requesting processor without having to satisfy severe interrupt timing constraint and Smith teaches one to balance each processor's workload by distributing the task according to the processor's current workload.

Referring to claim 4: Claim 1's argument applies; furthermore, since Smith teaches one to select the processor based on the workload; it can be any processor, including the one just causes the SMI.

Referring to claim 5: The admitted prior art discloses the processors' access to chip set's I/O port as one standard well-known system activities (Application, page 3, lines 8-9). Goodman also discloses that the processor writes to the memory (figure 1, structure 26) via the chip set's port (figure 1, structure 18).

Referring to claims 6-7: Both the admitted prior art (Specification, page 2, line 11) and Goodman (figure 1, structure 50) disclose the chip sets as a PCI bridge.

Referring to claim 8: The admitted prior art discloses the step of issuing from the expansion bridge the instruction causing the processor to enter the system management mode (Specification, page 2, lines 10-17). Goodman discloses that each of the processors of the system to enter system management mode (column 1, lines 50-54).

Referring to claim 16: The admitted prior art discloses issuing an instruction from a first processor of the system to a chip set (Specification, page 2, lines 10-11), receiving the instruction at the chip set and in response issuing a command causing the processors to enter system management mode (Specification, page 2, lines 12 and 18-19), writing parameters for the SMI routines to a predetermined register of a first processor (Specification, page 3, lines 4-6), and saving register contents of each processor to a memory space associated with each respective processor (Specification,

page 2, lines 22-24). The admitted prior art's parameters for the SMI routines are the claimed predetermined signature.

The admitted prior art further discloses that a different processor, other than the processor initiating the interrupt, may be selected for handling the interrupt (Specification, page 3, lines 13-16); thus, the admitted prior art discloses selecting from among the multiple processors a second processor as a system management interrupt handler and then transmitting the software system management interrupt to the selected second processor.

Neither the admitted prior art discloses selecting the second processor according to an arbitration scheme nor the admitted prior art discloses scanning the content of the memory for the selected second processor to process the interrupt.

Goodman discloses an interrupt handling method in a multiprocessor environment. Goodman discloses scanning the content of the memory for the selected second processor to process the interrupt (figure 4, steps 126, 128, and 130); and when the second processor locates the saved predetermined signature in one of the memory spaces associated with the processors of the computers system, using the contents of the memory space associated with the predetermined signature for any parameters necessary for the handling of the system management interrupt (figure 4, steps 134, 136, and 138). Goodman teaches one to identify the requesting processor without having to satisfy severe interrupt timing constraint (column 1, lines 66-67, column 2, lines 1-5). Although Goodman discloses and teaches one to scan the processor

register in handling interrupt, Goodman does not explicitly disclose an arbitration scheme in selecting one processor to execute the interrupt.

Smith discloses assigning tasks to the idle processor (abstract). Smith teaches one to distribute the task to the processor based on the processor's current workload.

Hence, it would have been obvious to one having ordinary skill in the computer art to adapt the teachings of Goodman and Smith onto the admitted prior art because Goodman teaches one to identify the requesting processor without having to satisfy severe interrupt timing constraint and Smith teaches one to balance each processor's workload by distributing the task according to the processor's current workload.

Referring to claim 19: The admitted prior art discloses the processors' access to chip set's I/O port as one standard well-known system activities (Application, page 3, lines 8-9). Goodman also discloses that the processor writes to the memory (figure 1, structure 26) via the chip set's port (figure 1, structure 18).

Referring to claims 20-21: Both the admitted prior art (Specification, page 2, line 11) and Goodman (figure 1, structure 50) disclose the chip sets as a PCI bridge.

Referring to claims 22-23: The admitted prior art discloses receiving at each processor an instruction that the system management interrupt has been issued (Specification, page 2, lines 19-20) and entering system management mode at each processor (Specification, page 2, lines 20-21).

The admitted prior art further discloses that a different processor, other than the processor initiating the interrupt, may be selected for handling the interrupt (Specification, page 3, lines 13-16); thus, the admitted prior art discloses selecting from



among the multiple processors a second processor as a system management interrupt handler.

But the admitted prior art does not disclose selecting the second processor according to an arbitration scheme. The admitted prior art also does not disclose scanning, locating, and retrieving the content of the memory for the selected second processor to process the interrupt.

Goodman discloses an interrupt handling method in a multiprocessor environment. Goodman discloses scanning the contents of the memory space associated with each processor (figure 4, steps 126, 128, and 130); and when the second processor locates the saved predetermined signature in one of the memory spaces associated with the processors of the computers system, using the contents of the memory space associated with the predetermined signature for any parameters necessary for the handling of the system management interrupt (figure 4, steps 134, 136, and 138). Goodman teaches one to identify the requesting processor without having to satisfy severe interrupt timing constraint (column 1, lines 66-67, column 2, lines 1-5). Although Goodman discloses and teaches one to select a processor to handle the interrupt, Goodman does not explicitly disclose an arbitration scheme in selecting the processor.

Smith discloses assigning tasks to the idle processor (abstract). Smith teaches one to distribute the task to the processor based on the processor's current workload.

Hence, it would have been obvious to one having ordinary skill in the computer art to adapt the teachings of Goodman and Smith onto the admitted prior art because

Goodman teaches one to identify the requesting processor without having to satisfy severe interrupt timing constraint and Smith teaches one to balance each processor's workload by distributing the task according to the processor's current workload.

### ***Response to Arguments***

Applicants' arguments filed 10/23/2006 have been fully considered but they are not persuasive.

At the outset, Applicants are reminded that claims subject to examination will be given their broadest reasonable interpretation consistent with the specification. *In re Morris*, 127 F.3d 1048, 1054-55 (Fed. Cir. 1997). As a matter of fact, the "examiner has the duty of police claim language by giving it the broadest reasonable interpretation." *Springs Window Fashions LP v. Novo Industries, L.P.*, 65 USPQ2d 1862, 1830, (Fed. Cir. 2003). Applicants are also reminded that claimed subject matter not the specification, is the measure of the invention. Disclosure contained in the specification cannot be read into the claims for the purpose of avoiding the prior art. *In re Sporck*, 55 CCPA 743, 386 F.2d, 155 USPQ 687 (1986).

With this in mind, the discussion will focus on how the terms and relationships thereof in the claims are met by the references. Response to any limitations that are not in the claims or any arguments that are irrelevant and/or do not relate to any specific claim language will not be warranted.

**The 103 Rejection:**

With regard to claims 1, 16, and 22, Applicants argue that:

Each of the independent claims of this application specifies that each processor of the computer system is both operable to process a system management and is **not dedicated** to

processing the system management interrupts of the computer system. The fact that each processor of the computer system is **not dedicated** to the processing of the system management interrupt is in contrast to the disclosure of the asserted prior art, including Goodman. The examiner has recognized in a previous office action that the processor of Goodman includes one processor that is **dedicated** to handling the interrupts of the computer system of Goodman:

Goodman discloses dedicating the boot processor to handle the interrupt management; the practice of Goodman's dedicating one processor to handle the interrupt management is the claimed selecting means.

(Office Action mailed 10/06/2005, page 8, paragraph 4). Thus, it is plain from the examiner's understanding of Goodman that Goodman involves dedicating one processor to the task of processing interrupts. In the present invention, however, it is specified that **none** of the processors are dedicated to the handling of the system management interrupt. This disclosure is not present in Goodman.

In response to Applicants' argument, while the Examiner agrees with Applicants that Goodman discloses dedicating the boot processor to handle the interrupt management, Applicants are reminded that the rejection is based on a combination of references. One cannot show nonobviousness by attacking references

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individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). Goodman is relied upon in the above 103 Rejection as Goodman discloses an interrupt handling method in a multiprocessor environment. Goodman discloses scanning the contents of the memory space associated with each processor (figure 4, steps 126, 128, and 130); and when the second processor locates the saved predetermined signature in one of the memory spaces associated with the processors of the computers system, using the contents of the memory space associated with the predetermined signature for any parameters necessary for the handling of the system management interrupt (figure 4, steps 134, 136, and 138). Goodman teaches one to identify the requesting processor without having to satisfy severe interrupt timing constraint (column 1, lines 66-67, column 2, lines 1-5).

Applicants also argue that:

This deficiency is not cured by either the allegedly admitted prior art or Smith. The allegedly admitted prior art does not explicitly or inherently teach or suggest that **none** of the processors is dedicated to processing the system management interrupts of the computer system. Additionally, Smith does not teach or suggest system interrupts, processing system interrupts, or that **none** of the processors are dedicated to processing system interrupts.

Because each of the elements of the claims is not present in the prior art of record, the rejection of the independent claims should be withdrawn, and these claims should be passed to issuance.

Contrary to Applicants' argument, as clearly set forth in the 103 Rejection, as disclosed in the acknowledged prior art, at least page 2, line 18 to page 3, line 21, none

of the processor is a dedicated processor dedicating to SMI. Rather, any one of the processors can be selected to handle SMI. Specifically, the acknowledged prior art further discloses that a different processor, other than the processor initiating the interrupt, may be selected for handling the interrupt (Specification, page 3, lines 13-16); thus, the admitted prior art discloses selecting from among the multiple processors a second processor as a system management interrupt handler. Note that to select is to choose in preference to another or others. Note also that selection must be based on specific criteria. Thus, it is clear that selection based on specific criteria is selection based on an arbitration scheme. In any event, as already indicated by Ex. King, the use of arbitration scheme in general is old and well-known as evidenced by at least Smith.

### ***Conclusion***

**THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

***Contact Information***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khanh Dang whose telephone number is 571-272-3626. The examiner can normally be reached on Monday-Friday from 9:AM to 5:PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart, can be reached on 571-272-3632. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



**Khanh Dang  
Primary Examiner**